What is claimed is:

1. A method of forming contact holes for a memory device, comprising the steps of:

providing a substrate having a memory array region and a peripheral circuit region, a plurality of gate structures formed overlying the array region and the peripheral circuit region, wherein the gate structure comprises a gate, a gate capping layer, and a gate spacer;

forming a first insulating layer between the gate structures;

forming a second insulating layer on the gate structures and the first insulating layer;

successively etching the second and first insulating layers using the gate capping layers, the gate spacers, and the substrate as stop layers to form bit line contact holes on the memory array region to expose the substrate and the gate spacers and form substrate contact holes and gate contact holes on the peripheral circuit region to expose the substrate and the gate capping layers;

forming a protective spacer over each sidewall of the bit line contact holes, the substrate contact holes, and the gate contact holes;

etching the gate capping layer under each gate contact hole using the protective spacer as a stop layer to expose the gate; and

removing the protective spacers.

2. The method as claimed in claim 1, further forming a hard mask on the second insulating layer.

3. The method as claimed in claim 2, wherein the hard mask is a polysilicon layer.

4. The method as claimed in claim 1, wherein the gate comprises a metal silicide layer.

5. The method as claimed in claim 1, wherein the gate capping layer and the gate spacer are silicon nitride layers.

6. The method as claimed in claim 1, wherein the first insulating layer is a borophosphosilicate glass (BPSG) layer.

7. The method as claimed in claim 1, wherein the second insulating layer is a tetraethyl orthosilicate (TEOS) oxide layer.

8. The method as claimed in claim 1, wherein the protective spacer is a metal nitride spacer.

9. The method as claimed in claim 8, wherein formation of the protective spacers comprises the steps of:

forming a conformable metal nitride layer on the second insulating layer and the inner surfaces of the bit line contact holes, the substrate contact holes, and the gate contact holes; and

anisotropically etching the metal nitride layer using the BCl, CL_2, HBr, and N_2 as reaction gases to form the protective spacers.

10. The method as claimed in claim 8, wherein the protective spacer is a titanium nitride layer.

11. The method as claimed in claim 10, wherein the protective spacer is removed by a mixture of sulfuric acid and hydrogen peroxide (SPM).

12. The method as claimed in claim 1, wherein the protective spacer has a thickness of about 80 to 200Å.

13. The method as claimed in claim 10, wherein the gate capping layer is etched using CH3F, O2, and CO as reaction gases.

14. A method of forming contact holes, comprising the steps of:

providing a substrate on which a plurality of gate structures is formed, wherein the gate structure comprises a gate, a gate capping layer, and a gate spacer;

forming an insulating layer on the gate structures and filling between the gate structures;

etching the insulating layer using the gate capping layers, the gate spacers, and the substrate as stop layers to form first contact holes between the gate structures to expose the substrate and the gate spacers and form second contact holes

overlying each gate structure to expose the gate capping layers;

forming a protective spacer over each sidewall of the first contact holes and the second contact holes;

etching the gate capping layer under each gate contact hole using the protective spacer as a stop layer to expose the gate; and

removing the protective spacers.

15. The method as claimed in claim 14, further forming a hard mask on the insulating layer.

16. The method as claimed in claim 15, wherein the hard mask is a polysilicon layer.

17. The method as claimed in claim 14, wherein the gate comprises a metal silicide layer.

18. The method as claimed in claim 14, wherein the gate capping layer and the gate spacer are silicon nitride layers.

19. The method as claimed in claim 14, wherein the insulating layer comprises borophosphosilicate glass (BPSG).

20. The method as claimed in claim 14, wherein the insulating layer comprises tetraethyl orthosilicate (TEOS) oxide.

21. The method as claimed in claim 14, wherein the protective spacer is a metal nitride spacer.

22. The method as claimed in claim 21, wherein the formation of the protective spacers comprises the steps of:

forming a conformable metal nitride layer on the insulating layer and the inner surfaces of the first contact holes and the second contact holes; and

anisotropically etching the metal nitride layer using BCl, CL_2, HBr, and N_2 as reaction gases to form the protective spacers.

23. The method as claimed in claim 21, wherein the protective spacer is a titanium nitride layer.

24. The method as claimed in claim 23, wherein the protective spacer is removed by a mixture of sulfuric acid and hydrogen peroxide (SPM).

25. The method as claimed in claim 14, wherein the protective spacer has a thickness of about 80 to 200Å.

26. The method as claimed in claim 14, wherein the gate capping layer is etched using CH3F, O2, and CO as reaction gases.